SOME RELIABILITY PROBLEMS OF ELECTRONIC PACKAGES

Titu-Marius I. Băjenescu, prof. dr.Eng.
Switzerland

1. INTRODUCTION

During the last few years the use of electronic-based devices has been playing an increasingly relevant role in our day-to-day life. In order to hinder the strong competition in this market, the performance requirements have been following the same trend. The competitive pressure to produce "*smaller, faster, cheaper*" microelectronic devices means that reliability must be achieved using only the minimum amount of material, and also the minimum amount of testing. Actual testing of complete devices is the most definitive means to find out whether a design is reliable, and also the slowest and most expensive. That is why failure[1] of microelectronic devices has become in this last decade a prominent field of research. A "*physics of failure"* approach based on a scientific determination of the dominant failure mechanisms and failure sites within the component is generally accepted. The results of this physics of failure analysis allow a designer to choose package geometries and materials which reduce the risk of failure by the identified mechanisms. This makes reliability assessment a part of the design process rather than just a tool for predicting the useful life of an existing product. A technically and economically relevant branch of electronic devices is constituted by the so-called electronic packaging that is when the circuitry is permanently plastic encapsulated or inserted in a ceramic housing. The introduction of new equipment and techniques in the assembly process has had a tremendous impact on device reliability. Automated wire bonding machines have produced more consistent wire bonding quality and improved productivity.

2. IC PACKAGE

The IC package was born of the IC, which, though it had great potential power within, did not have the ability to easily communicate with the World beyond owing to the fine and seemingly random pitch of its contacts. Chip scale packaging (CSP) represented the next step in the evolution of packaging. It was fundamentally an effort to obtain the benefits of flip chip assembly (smallest form factor, highest performance, etc.), but without all of the risks and challenges, and with the benefit of standards, which is virtually impossible with flip chip. However, CSP technology has not replaced flip chip technology but has instead augmented it. The last stop in chip scale packaging is chip size, and that has been accomplished. The need to move large quantities of data at high speeds continues to increase, pressuring component manufacturers to improve their technology and, simultaneously, to reduce costs. One of the key factors in both cost and performance is packaging. Wireless IC and component packaging is undergoing substantial changes in response to these pressures. Reliability aspects are of extreme importance for assembly and packaging, which has become a limiting factor for both cost and performance of electronic systems. On the one hand reliability can be negatively influenced by modern front-end and packaging technology, on the other hand new applications and corresponding field requirements can result in the need for new reliability tests e.g. for mobile devices. Today the three main package trends for mobile devices towards ongoing miniaturization and higher system integration are ball grid array type packages, leadless packages, and wafer level type packages. For the future it is necessary that test conditions must follow the field requirements to guarantee optimum reliability results. The value of a packaging solution - in both cost and performance - increases as the frequency of operation increases, becoming a dominant factor for product success at frequencies above 2 GHz. Failure to obtain a packaging solution that meets both performance and cost criteria can contribute to late product introduction or even total market failure [1].

2.1 IC packaging technologies

The new *IC packaging technologies* evolves towards packaging at wafer level including wafer-level burn-in and test, and system-in-package (SIP)

[1] Failure consists of a transition from reliable to failed states. Irrespective of the specific mechanisms, failure virtually always begins through a time-dependent movement of atoms, ions, or electronic charge from benign sites in the device or component to harmful sites. If these atoms or electrons accumulate in sufficient numbers at harmful sites, damage ensues.

or three-dimensional packaging of ICs, respectively.

Systems packaging to system on package (SOP) developed more or less from the traditional board packaging with discrete components assembled by surface-mount technology (SMT) processes. Now the predictable future trends are towards nano-packaging for nano-systems [2]. The transition is towards nano chips, with less than 100 nm features.

To control a manufacturing process means to keep in time the quality of this process, to assure the reliability of the process. The operations that must be made are evaluation, optimization, qualification and monitoring. An optimal process is first qualified and then, with the aid of the monitors, the process can be kept under control.

Packages typically include a chip (called also die), which contains the primary circuit elements; the chip is composed by many elementary cells. Other elements are die attach, lead frame, leads, wires, substrate, passive elements, substrate attach, wire bonds, interconnection wiring and case (Figure 1A). The die is attached to substrate by a die attach composed usually of gold, epoxy, polyimide or solder alloy. The substrate provides the mechanical support to the die and acts as heat carrier to the package case. Failure occurs typically when the intermediate dielectric cracks, thus allowing for leakage currents. These latter's are measured by applying a voltage bias across bond pads of structure of interest [3].

2.2 Polymers

Among various materials, polymers are widely used in microelectronics as different product constituents, such as encapsulants, conductive or non-conductive adhesives, underfills, moulding compounds, insulators, dielectrics, and coatings. The behaviour of these polymer constituents determines the performance, such as functionality and reliability of the final products. Therefore, the successful development of microelectronics depends to some extend on the optimal design and processing of polymer materials. Due to the development trends of microelectronics – characterized mainly by ongoing miniaturization down to nano scale – technology and functionality integration, eco-designing, shorter-time-to-market, the development and application of polymers becomes one of the bottlenecks for the microelectronic industry. With the development and introduction of new packaging materials there are many new requirements to packaged device reliability. Most of these new materials require extensive characterization, due to the lack of historical reliability data [4].

2.3. Passivation in plastic packages

Passivation is the final layer on the die.
Passivation has two main functions:

(i) Moisture barrier

• Moulding compound is not a moisture barrier.
• Silicon oxides are not good moisture barriers.
• Plasma-enhanced chemical vapour deposition (PECVD) silicon nitride or silicon oxynitride film is a good barrier.
• Film must be thick enough to avoid pinholes, coverage defects.

(ii) Mechanical protection

• Silicon nitride films are brittle.
• Polyimide compliant film protects silicon nitride.
• Polyimide can react with moisture (depending on formulation).

2.4 Reflow soldering

Reflow soldering such as vapour phase (VP) soldering or infrared (IR) soldering for soldering surface mounted devices (SMD) onto printed circuit boards (PCBs). During the process, packages are heated up above solder melting temperature. If the plastic encapsulant has absorbed moisture, package cracking may occur during reflow soldering. Cracking must be prevented to guarantee the reliability of mounted devices. Cracks are caused by vapour pressure generated inside the package causing excessive stress in the plastic [6]. Package cracking occurs as follows: *(i)* Moisture absorption process: Atmospheric moisture dissolves and diffuses in the plastic encapsulant. *(ii)* Vaporization process: Moisture at the interface between the chip pad and the plastic is vaporized by heating during reflow soldering. The vapour pressure deforms the plastic below the chip pad and causes stress in the plastic. If the stress is excessive, package cracking occurs [7].

2.5 Package cracking

For the evaluation of package cracking which occurs in SMDs that have absorbed moisture, a moisture diffusion analysis in the plastic, a deformation and stress analysis of the package and measurement of the some properties of plastic of high temperature were performed in [7]. The validity of the analysis is confirmed by a measurement of deformation of packages which

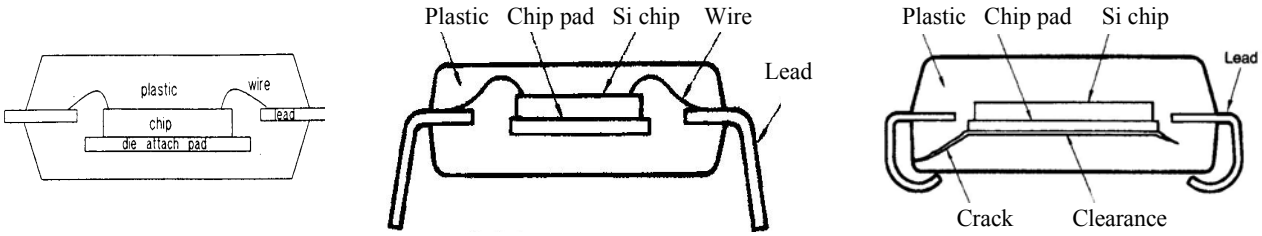

Figure 1. a) Scheme of a plastic encapsulated device [5]. **b)** Structure of insertion type [7]. **c)** Package cracks (after [7]).

area heated by IR. Vapour pressure and distribution of moisture content are calculated with the aid of the analytical model represented in figure 2 which have permitted to evaluate quantitatively package cracking.

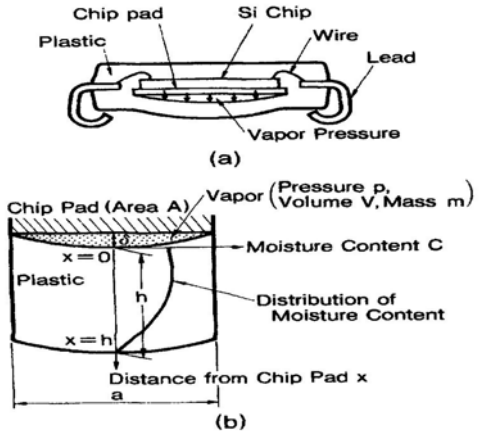

Figure 2. Analytical model (after [7]).

3. CLASSIFICATION OF FAILURES

Failures in microelectronic devices are often classified into electrical, mechanical, and corrosion failures. The mechanical ones normally cause the loss of device functionality well before the visible breaking of the device. In Figure 3 is given a detailed summary of possibly failure-affected parts in electronic devices and the related mechanisms. One can see that in the majority of cases the failure is clearly due to fatigue and/or fracture. Heat generated by Joule's effect during transient and steady-state conditions causes a mismatched thermal dilatation between the many different materials fit together and the repeated on-off operation originates thermo-mechanical fatigue and a subsequent cracking phenomenon. Furthermore, in plastic encapsulated devices initial residual stresses are induced by the packaging resin shrinkage after cooling due to assembly-resin mismatch. The same kind of problem can be found in the reflow soldering process, where hot (up to 250°C) air is used to melt the solder.

3.1 How to accelerate failure

Specification of the product testing or operating conditions is essential in predicting reliability. For example elevating temperature is the universal way to accelerate failure. It therefore makes a big difference whether the test temperature is 25°C, -25°C, or 125°C. Similarly, other specifications might be the level of voltage, humidity, etc., during testing or use. A key quantitative measure of reliability is the failure rate[2]. This is the rate at which a device or component can be expected to fail under known use conditions. Such information is important for both manufacturers and purchasers of electronic products. Each failure mode could, in principle, be caused by one or more different failure mechanisms. The latter are the specific microscopic physical, chemical, metallurgical, environmental phenomena or processes that cause device degradation or malfunction.

3.2 Failure mechanisms

The dominant failure mechanisms are a function of the package geometry, architecture and materials, and of accelerating environmental (temperature, relative humidity, pressure and static charge and their cycles, gradients and transients) and operational stress (voltage and current). Failure mechanisms occurring predominantly at the die level include slow trapping, hot electrons, electrical overstress, electrostatic discharge, dielectric failure, oxide breakdown, and electromigration. First level failure mechanisms generally arise from corrosion, differential thermal expansion between bonded materials, large time-dependent temperature changes, and large spatial temperature gradients, all

[2] Because failure rate is not a precise engineering parameter, it is important to be aware of the severe limitation of a reliability prediction based upon a 'parts count' model. The measured failure intensity of a component is seldom due to a single repeatable process. It is most frequently attributable to many physical, chemical and human processes and interactions.

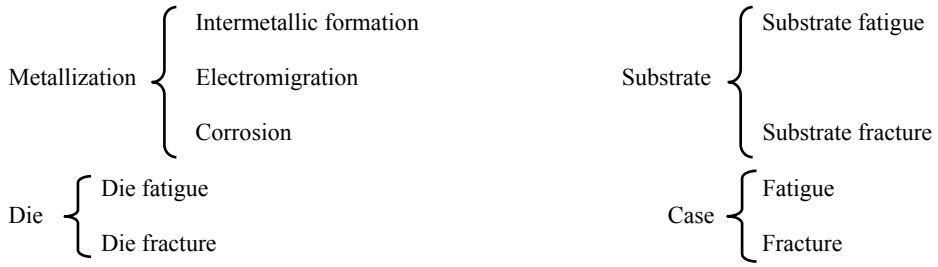

Figure 3. Possible failure-affected parts and the related failure mechanisms in microelectronic packaging.

3.3 Packaging related failure mechanisms (FMs) (see too Tables 1 and 2)

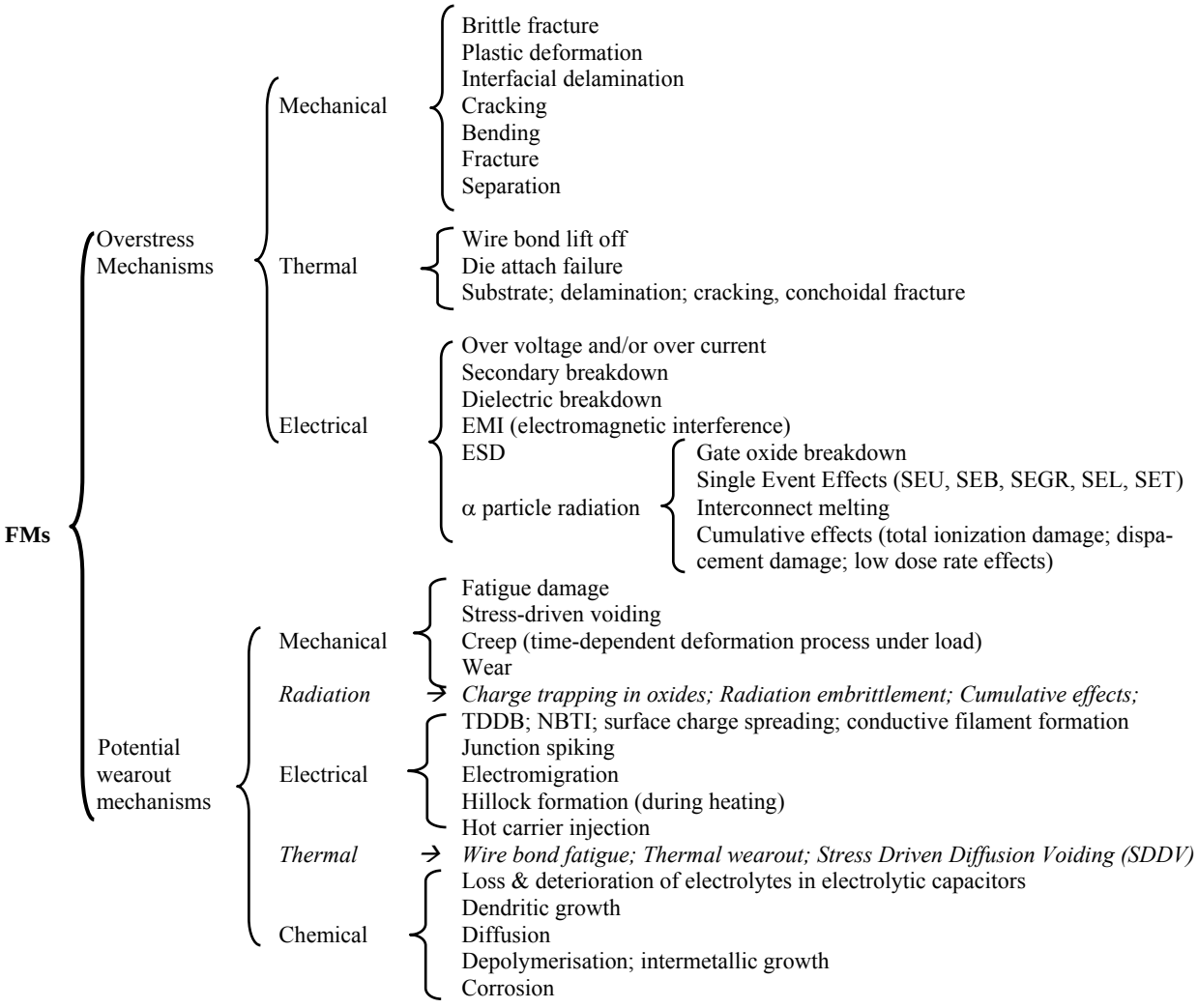

Figure 4. Taxonomy of failure mechanisms in microelectronics packaging.

of which can cause tensile, compressive bending, fatigue, and fracture failures.

4. CORROSION

The corrosion is the most prevalent mechanism since polymers have non-zero moisture uptake. It consists of *(i)* anodic reactions (oxidation reactions in which a metal loses electrons) and *(ii)* cathodic reactions (reduction reactions in which the lost electrons combine with another species). It depends on the thermodynamic stability of the metal (Au is the most stable of metals relevant to packaging).

Moisture-induced cracking during solder reflow is a critical reliability problem with plastic-encapsulated microcircuits (PEMs). Such cracking,

referred to as “popcorning” occurs from the evaporation and expansion of moisture absorbed by the moulding compound. The study [8] is aimed at establishing a rule-based system to address reliability problems related to popcorning such as interfacial delamination, mold compound moisture sensitivity, and mold compound fracture toughness.

4.1 Corrosion influence

The interfacial shear (IS) force of copper ball into Al-based bond pad depends on the formation and growth of Cu-Al intermetallic. Surface analysis of ball-peeled bond pad using XPS indicated that the cracks were due to stress corrosion cracking at Al that have been stimulated by Cu. The results of study [9] indicated that the Cu-Al bonds have been weakened by stress corrosion cracking at outer bond interface and reduce the IS force.

4.2 Corrosion mechanisms in microelectronic packaging

Microelectronic packaging systems are constructed from a wide range of materials. They make use of almost all major kinds of materials, such as metals, alloys, polymers, ceramics and fibres. Corrosion-induced failures in microelectronic packaging become more significant when the feature sizes become smaller and smaller, because small features are more sensitive to corrosion-induced failure. Corrosion involves essentially electrochemical processes except for those oxidised at the elevated temperature and in the dry environment. The basic requirements for electrochemical corrosion include electrically conductive anode, cathode, interconnecting electrolyte (humidity environment) and driving force. The driving force for electrochemical corrosion is the difference of electrochemical potentials between anode and cathode. The driving force can result from coupling of two dissimilar materials, concentration gradient or externally applied electrical bias. Any corrosion reaction must be analysed from two aspects: its thermodynamic feasibility and its kinetics. Driving force gives the thermodynamic feasibility, and kinetics is determined by the variables of the system. The electrochemical corrosion kinetics (rate) depends on a number of factors which include the area ratio of anode to cathode, the polarisation resistance of anode and cathode, conductivity of electrolyte solution, solution pH value, temperature, contamination, and driving force. Small anode and big cathode system corrodes much faster than big anode and small cathode. This is the case for the active metal coated with noble metal. For instance, gold is deposited onto aluminium pad to prevent aluminium from corrosion. If defects of deposit gold layer exist and small area of fresh aluminium is exposed to the corrosive environment, aluminium is corroded much faster because of small anode of exposed aluminium and big gold deposit layer around. Another example is paint coated aluminium wire. Polarisation occurs when a current passes through an electrochemical system. There are three types of polarisation phenomena such as resistance polarisation, concentration polarisation and electrochemical activation polarisation. For those metals or alloys with stable protective oxide/hydroxide layers formed on their surface, the resistance polarisation is very significant and their corrosion rate may be very low due to the high resistance (R) in the electrochemical cell. This is basically how corrosion resistant metals and alloys such as stainless steels, nickel and its alloys, copper and its alloy, work well in some corrosive environment. Halide ions such as chloride, bromide are good depolarisers to break the stable oxide/hydroxide layer and reduce resistance polarisation. The resistance polarisation can also be caused by poor conductivity of the electrolyte solution. Concentration polarisation occurs when there exists concentration difference between around electrode and inside the solution or concentration difference at difference sites of the electrode. The consequence of concentration polarisation will yield potential difference due to concentration gradient.

4.3 Concentration gradient corrosion

Corrosion due to concentration gradient is controlled by diffusion of reacts and products in the electrolyte. For electrochemical activation polarisation, it relates to the rate determining step for an electrochemical reaction process. For example, Al-Au galvanic couple in the electrolyte solution, Al acts as anode and Au acts as cathode. Aluminium loses electrons to be oxidised and these electrons are transferred to gold cathode. Electrons will be accumulated at the cathode, if the cathode reduction reaction is very slow because it needs higher activation energy. The consequences of the activation polarisation in this case will change the cathode reduction potential to more negative and slow the corrosion rate.

Hydrogen evolution reaction and oxygen reduction reaction are two-cathode-depolarisation reactions. In microelectronic devices

Table 1. Packaging related failure mechanism and countermeasures (after [10]).

Failure mechanism	*Countermeasures*
Brittle fracture	Minimise stress defects and/or flaws
Plastic deformation	Minimise stress and use better materials
Interfacial deformation	Improve adhesion
EMI (el. magn. interference)	Apply shielding layer
ESD (el. static discharge)	Improve circuit design, use ground tools
Gate oxide breakdown	Lower voltage and improve oxide layer
Interconnect melting	Reduce current density
α particle radiation induced signal error	Use better material
Fatigue fracture	Minimise stress/strain/temperature and use alternate materials geometry and dimensions
Creep	Minimise stress and use refractory materials
Wearout	Minimise stress and use harder materials
Stress-induced voids	Minimise stress
Open- or short-circuit caused by electromigration	Reduce current density and use alternate material, i.e. copper
Short-circuit caused by junction spiking	Improve process and use metal buried layer
Corrosion	Provide sealing and encapsulation
Diffusion	Lower temperature and use diffusion barrier
Dendritic growth	Increase thickness and reduce humidity

and their packaging, there are three major types of corrosion.

They are galvanic corrosion, pitting and stress corrosion crack. Since aluminium and its alloys are the most widely used metal and corrosion of aluminium is one of the commonest problems in microelectronic devices and packages, aluminium is used as an example material for describing and discussing corrosion mechanisms.

4 .4 Galvanic corrosion

Galvanic corrosion is also called dissimilar metal corrosion. Basically it refers to a corrosion phenomenon induced when two different metals or alloys are coupled in a corrosive electrolyte. When two dissimilar metals or alloys are brought into electrical contact under electrolyte such as water with ions, one of the metals or alloys with lower electrochemical reduction potential acts as anode and corrodes faster than its natural corrosion while the other one with higher electrochemical reduction potential acts as cathode and corrodes slower than its natural corrosion or even is stopped from corrosion. Galvanic corrosion can also occur in an alloy with multiple phases such as aluminium-copper alloy. Different phases have different electrode potentials, which results in one phase with lower electrode potential acting as anode and being selectively corroded. In the microelectronic packaging, the commonly used metals or alloys are aluminium, copper, gold, silver, tin, lead, nickel and their alloys. There are lots of places involving two-dissimilar metals electrical contact together such as die pad (Al/Cu), wire to die pad bond (Au/Al), bump metallisation (Al/Ni/Cu, Al/Ti/Cu, Al/Pd/Cu, Al/Zinc/Ni) for flip chip. Aluminium is more active than tin; if aluminium and tin contact together in an electrochemical system, aluminium acts as anode and tin acts as cathode.

5. POPCORNING

Popcorning during solder reflow is driven by evaporation of absorbed water into interfacial defect void. Due to lack of data, the steam pressure during popcorning has been assumed as a single value, normally some fraction of the steam saturation pressure at a convenient temperature in popcorning models. A new experimental and analysis methodology to determine the engineering rate of water evaporation from polymer is described in paper [11]. Using the proposed method, evaporation rate from immersed epoxy is measured. Comparison of the measured rate with a conventional approximation of water evaporation, the conventional approach was found to overestimate the measured rate by nearly two orders of magnitude. To prevent popcorning, the actual evaporation rate can be used in process design as well as material selection of polymer materials.

The study [12] analyses the popcorning effect of PBGA packages using the method of fracture mechanics. The following three specific problems are studied: *(1)* crack initiation in the die attach of

the package, *(2)* crack growth in the die attach, and *(3)* crack growth at the interface between the solder mask and copper. Two different methods (crack tip opening displacement and virtual crack closure technique) are used to determine the crack-tip parameters such as the strain energy release rate, stress intensity factors, and phase angle for different crack lengths and temperatures.

6. PRESENCE OF HUMIDITY

All polymers are permeable to moisture and hence some water will inevitably be present at the surface of the IC (Figure 5). However this moisture does not automatically result in damage to the IC. Other constituents such as ionic contamination and high temperature must be present to enable known failure modes.

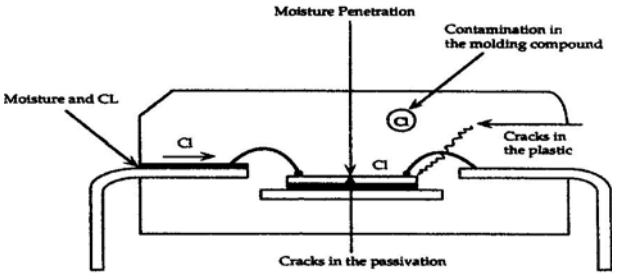

Figure 5. Mechanism of moisture related problems (after[19]).

6.1 High humidity environment

Lead frame is the primary package metallurgical bond pad interface in microelectronic devices which provides external interconnection. The most predominant lead frame material is copper with tin plating. Over the years, galvanic corrosion and copper oxidation are two main reliability concerns for any microelectronics packages with copper lead frame, when operating under high humidity environment; often, this observation is correlated to the rise in drain-to-source on-resistance. Failure analysis result revealed that non-homogeneous tin plating is the contributing factor. In the past, the operators utilised conventional cleaning method, that is, polished leads backside with sandpaper followed by acetone rinse. Nevertheless, this could not remedy the problem effectively. The author of paper [13] has performed research study to prove that solder dip is a better solution to eliminate corrosion and oxidation away from the leads.

7. HIGH MECHANICAL STRESS

Another concern in commercial IC packaging is the occurrence of high mechanical stress at the IC surface as a result of differential thermal contraction of mould compound and IC die as the part cools from the moulding and curing temperatures to ambient. Excess stress can produce cracking or damage to metal conductors on the IC surface. In addition, some circuits such as analog are susceptible to stress induced shifts in certain circuit parameters. The measurement and control of packaging related stresses is a major issue in some areas of packaging. Table 2 resumes the package related failure modes and mechanisms; Table 3 summarizes the die-related failure modes and mechanisms.

8. NEW FAILURE MECHANISMS

New failure mechanisms affecting the packages arise due to internal mechanical stresses. Static low temperature levels cause the maximum electromechanical stress for TCE mismatches, because of residual stressing occurring after die packaging. This can result in brittle die cracking, especially in GaAs, if the critical crack length has been reached. Fatigue phenomena affect basically materials like metals or alloys with low melting temperatures [14].

9. HIGH DENSITY PACKAGES

Much of the mechanical evaluation done has focused on simple techniques such as wire pull testing with simple pass / fail criteria based on the failure force. The continued drive towards ever smaller, faster, and cheaper microelectronic devices driven by the market for mobile phones, PDA, laptops and MP3 players has lead to the development of very high density packages. At the same time, environmental legislation is driving changes in some of the established materials e.g. lead free solders and process redesign to reduce process waste. A cross section of a typical high density ball grid array (BGA) package is shown in Figure 6.

10. PACKAGE RELATED DEFECTS

The package provides the physical support for the microdevice and enables electrical connection to be made to the external circuitry; it serves also to

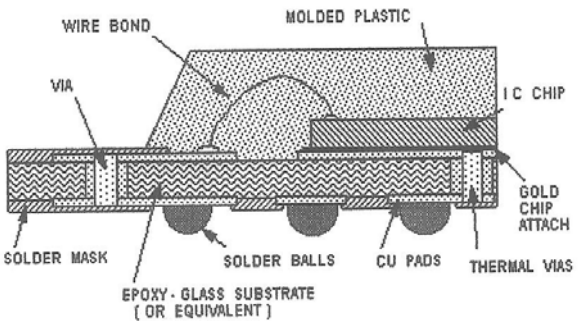

Figure 6. Cross section of BGA package showing interfaces between dissimilar materials (after [15]).

provide electrical and mechanical protection for the microdevice, and hence must be present an inert and dry atmosphere to the surface of the semiconductor, and must give protection against mechanical and thermal shock. Each element of the packaging process provides some form of protection for the device. The electrical failures are commonly due to some form of corrosion which may be related to the integrity of the surface passivation layer or the hermeticity of the external package. Mechanical failures arise from the mishandling of the device, or physical shock resulting in a breakage of the device [16].

11. GREEN PACKAGE INITIATIVE

With the push from semiconductor manufacturers for complete green IC packaging growing and becoming a global initiative, assembly and test providers must find the right combination of green IC package materials. For each package material component the green alternatives must be evaluated and the challenge of using these new materials must be overcome to meet the reliability demands of IC manufacturer.

Challenges: For substrate: Cost, supply, and standardisation. For mold compound: Survives delimitation of Pb-free reflow temperatures by increasing the adhesion of the mold compound. Make the optimisation of mold process and/or of material properties. Lead finish counter-measures: Post-plate reflow tin over nickel; optimising plating bath chemistry; annealing. Regarding the die attach, there are several considerations when choosing the best die attach material to match the other halogen-free components (low stress on the die, high thermal stability, minimal bleed-out, low moisture absorption) [17].

Findings from the laboratory tests include age related conditions (heat damage or burnt wire, evidence of arcing, chafing, delamination, and breaches at hot stamp areas). Based on frequency of findings, the most common wire condition anomalies are heat damage or burnt wire, vibration damage/chafing and cracked insulation.

In modern IC parts, ionic contamination is reduced to extremely lower levels in both the wafer fabrication and plastic moulding operations. As a result, corrosion of conductors in commercial ICs is extremely rare. However, it is possible to cause circuit damage and even failure by using very high temperatures, humidities, and bias voltages in accelerated temperature humidity bias (THB) test. A pressurized THB test run at a temperature above boiling point of water is referred to as highly accelerated stress test or HAST. On common commercial parts, a HAST at 160°C and 85% RH will produce measurable failures in 100's test hours. Hence THB tests cannot be used to "screen" PEMs although they are very useful as both sampling test and a method to evaluate materials and processes.

The focus of concern in commercial manufacturing has shifted to issues associated with sudden moisture release during high temperature solder reflow during mounting of the ICs to the PC board. This so called "popcorn" effect can cause cracking in the package or delamination of interfaces inside the package. Although cracking and delamination do not usually produce a functional failure of the device, they are potential long term reliability issues.

Table 2. Package related failure modes and mechanisms.

Failure mode	***Failure mechanism***
Open	- Disconnection of bond wire or peeling - Stress due to oxidation or absorbed moisture and heat stress; Lead dirtiness
Soldering defect	- Surface oxidation or contamination
Shorts or leaks, Package cracking	- Wire touching (contact between the wires, chip and lead frame) - Electrochemical migration between leads - Delamination between the chip or lead frame and mold resin

Table 3. Die-related failure modes and mechanisms.

Failure mode	*Failure mechanism*
Open	• Aluminium wiring disconnection (corrosion, migration, latch-up) • Bonding pad corrosion • Polysilicon wiring disconnection (melting) • Bond peeling (formation of Au-Al and other intermetallic compounds)
Shorts or leaks	• Oxide film breakdown or pinhole • Electrostatic breakdown • *pn* junction degradation • Interlayer insulator breakdown or pinhole • Conductive foreign matter • Contamination within the process • Chip cracking • Entry of moisture
IC function failure (characteristic fluctuations and function failure)	• Hot electron or hot carrier injection to the oxide film • Surface inversion • Crystal defect • Contamination within the process
Malfunction	• Soft error • Latch-up • Electromagnetic interference (EMI)

The presence of humidity in the moulding compounds of non-hermetic surface mounted devices before assembling may have catastrophic consequences; during solder reflow, moisture which is present at the interface between mold and die-pad vaporizes and expands creating an internal stress which can result in either a crack in the plastic (popcorn effect), in interfacial delamination, or even in die cracking. The problem is usually solved using dried devices or providing a short temperature storage of the device immediately before assembling.

12. EVALUATING THE RELIABILITY

Twenty-first-century reliability culture must adapt to the paradigm that states “if a system operates as required for a required period without failure, it has meet an acceptable target of reliability” [18].

Traditionally one of the methods of evaluating the reliability of an electronic component or assembly has been thermal cycling; however the nature of this method means that it is very time consuming and is ill-suited to the short product and process development cycles associated with the first moving world of microelectronics. Various types of mechanical test e.g. cyclic fatigue and creep-fatigue on solder joints and assemblies can be used to augment or even replace thermal testing.

Scanning acoustic microscopy has been successfully implemented for the non-destructive detection of cracks and delaminations in integrated circuit packages. The incorporation of scanning acoustic microscope inspections in reliability tests of moulded surface mount components has identified delamination at the mold compound/die interface as the primary cause of electrical failure during temperature cycling. The ability of the acoustic microscope to non-destructively image stress distributions prior to failure would greatly extend the impact of scanning acoustic microscopy on new package development and process control. This may be particularly important for the packaging of devices with fragile low-k (dielectric constant) layers in the device structure.

13. CONCLUSION

The last years have brought about revolutionary changes in electronics technology in general and plastic packaging in particular. Hundreds of studies have reported progress in plastic package integrity brought about by improvements in materials, increased purity of the plastics, high quality passivation layer processes, high shock resistance, greater availability, lighter weight, lower acquisition costs, and major device manufacturer's quality programs. Tests for plastic devices, to accelerate known and possible failure mechanisms of PEMs,

must be developed, validated, and standardized. Improvements in encapsulated materials such as: low ionic impurities, low moisture adsorption, better adhesion properties, matching of thermal coefficients to die/lead frame, high glass transition temperature, higher thermal conductivity; and advances in passivation such as: better adhesion to die, less pinholes or cracks, low ionic impurity, lower water vapour absorption, thermal properties better matched to substrate, have caused dramatic improvements in the reliability of PEMs over the last several years.

References

1. Băjenescu, T.-M. and Marius Bâzu. *Mecanisme de defectare ale componentelor electronice, Matrix Rom, Bucharest, 2012.*

2. Băjenescu, T.-M., and Marius Bâzu. "*Packaging and Microfabrication of MEMS," Proceedings of 3rd International Conference on Telecommunications, Electronics and Informatics, May 20-23, 2010, Vol. 1, pp. 87-92.*

3. Băjenescu, T.-M., and Marius Bâzu. *Component Reliability for Electronic Systems, Artech House, Boston and London, 2010.*

4. Bâzu, Marius, and T.-M. Băjenescu. *Reliability Issues of Epoxy Materials Used in Microtechnologies. Proc. of 3rd Internat. Colloque PLUMEE 2013, Bacău, May 2013.*

5. Pendse, R. D. *A Comprehensive Approach for the Analysis of Package Induced Stress in ICs Using Analytical and Empirical Methods. IEEE Trans. Comp., Hybr. and Manuf. Tech., Vol. 14, No. 4, pp. 870-873.*

6. Fukuzawa, I., et al. *Moisture Resistance Degradation of Plastic LSI's by Reflow Soldering. Proc. of Internat. Rel. Physics Symp. 1985, pp. 192-197.*

7. Kitano, M., et al. *Analysis of Package Cracking During Reflow Soldering Process. Proc. 26th Internat. Ann. Reliab. Phys. Symp., pp. 90-95,ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber = 23432.*

8. Kuo, A. Y., et al. *Popcorning - A Fracture Mechanics Approach. Proceedings of the 46th Conference on Electronic Components and Technology, 1996, pp. 869-874.*

9. Tan, C. W., A. R. Daoud, and M. A. Yarmo. *Corrosion Study at Cu-Al Interface in Microelectronics Packaging. Applied Surface Science, 191 (2002), pp. 67-73. http://202. 127. 1.11/ass/191/19110.pdf*

10. Chen, W.-K. (ed.) *VLSI Handbook, Second Edition, Boca Raton: CRC Press, 2007, p. 8-8.*

11. Chong, J. I.-T., D. C. C. Lam, and P. Tong. *Measurement of Water Evaporation Rate for Popcorning. Proceedings of the International Symp. on Advanced Packaging Materials: Processes, 2000, pp. 131-134.*

12. Low, J. H., and W. R. Lee. *Temperature-Dependent Popcorning Analysis of Plastic Ball Grid Array Package During Solder Reflow With Fracture Mechanics Method. J. Electron. Packag., Vol. 122 (2000), Issue 1, p. 34.*

13. Seng, Y. L. *Reliability of Microelectronic Packages with Tin-Plated Copper Leads under High Humidity Operating Environment. Proceedings of 8th Electronic Packaging Technology Conference, 2006, EPTC, pp. 894-899.*

14. Ciappa, M. *Package Reliability in Microelectronics: An Overview. Proc. of First International Workshop on Electronics and Detector's Cooling, Weldec.*

15. McEnteggart, J., et al. *Characterisation of interfacial cracking in microelectronic packaging. www.instron.com/wa/library/Stream File.aspx?doc.*

16. Wood, J. *Reliability and Degradation of Silicon Devices and Integrated Circuits. in Reliability and Degradation, Howes, M. J.*

17. Toriaga, A. *Green IC Packaging: Options, Challenges and Direction. http://www. analogzone.com/grnt1213.pdf*

18. Pascoe, N. *Reliability Technology, John Wiley, Chichester, 2011.*

19. Reliability Analysis Center. *Plastic Microcircuit Packages: A Technology Review. www.dtic.mil/dtic/tr/fulltext/u2/a278419.pdf, p. 238.*

Recommended for publication: 02.10.2014.